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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2673	8

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/049,583	Applicant(s) TANAKA ET AL.	
	Examiner Prabodh M Dharia	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04-15-2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,43,44,47-49,52-58 and 64-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,43,44,47-49,52-58 and 64-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 52-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida et al. (6,496,170 B1).

Regarding Claim 52, Yoshida et al. teaches a display apparatus (Col. 3, Line 28) for conducting a display (Col. 3, Lines 28,29) by controlling a voltage applied to a display medium

with a potential of pixel electrodes (Col. 3, Lines 54-65) and applying voltages with both positive and negative polarities to the display medium (Col. 7, Line 55 to Col. 8, Line 6), wherein a capacitive coupling voltage is superimposed on the pixel electrodes from electrodes other than pixel electrodes 9Col. 12, Lines 55-64), and a distribution of the capacitive coupling voltage is made different in a display region between a case where a positive voltage is applied to the display medium and a case where a negative voltage is applied thereto (Col. 11, Lines 57 – 67, Col. 12, Lines 55-64, Col. 8, Lines 55 to Col. 9, Line 37).

Regarding Claim 53, Yoshida et al. teaches the electrodes other than the pixel electrodes are common electrodes (Col. 8, Lines 55-65).

Regarding Claim 54, Yoshida et al. teaches a display apparatus (Col. 8, Line 39) comprising: a plurality of pixel electrodes (Col. 6, Line 48) arranged in a matrix (Col. 6, Line 36); switching elements connected thereto (Col. 6, Line 42); scanning electrodes (Col. 6, Lines 64, 23-25), video signal electrodes (Col. 7, Line 5-7, Col. 6, Lines 25-27); common electrodes (Col. 6, Line 55,56); a counter electrode (Col. 6, Lines 55,56, Lines 12,13); a display medium interposed between the pixel electrodes and the counter electrodes (Col.6, Lines 9-16); and storage capacitance formed between the pixel electrodes (Col. 6, Lines 54-57, Col. 7, Lines 14-26) and the common electrodes (Col. 6, Lines 55-56), wherein a capacitive coupling voltage from the scanning electrode, and a capacitive coupling voltage from the common electrode are allowed to have a distribution in a screen (Col. 8, Lines 55-65), whereby flickering and a

brightness gradient are corrected simultaneously (Col. 11, Lines 57 –67, Col. 12, Lines 55-64, Col. 8, Lines 55 to Col. 9, Line 37).

Regarding Claim 55, Yoshida et al. teaches a display apparatus (Col. 8, Line 39) comprising: a plurality of pixel electrodes (Col. 6, Line 48) arranged in a matrix (Col. 6, Line 36); switching elements connected thereto (Col. 6, Line 42); scanning electrodes (Col. 6, Lines 64, 23-25), video signal electrodes (Col. 7, Line 5-7, Col. 6, Lines 25-27); common electrodes (Col. 6, Line 55,56); a counter electrode (Col. 6, Lines 55,56, Lines 12,13); a display medium interposed between the pixel electrodes and the counter electrodes (Col.6, Lines 9-16); and storage capacitance formed between the pixel electrodes (Col. 6, Lines 54-57, Col. 7, Lines 14-26) and the common electrodes (Col. 6, Lines 55-56), and the scanning electrodes of the stage concerned and the pixel electrodes (Col. 6, Lines 40-47), wherein a capacitive coupling voltage from the scanning electrode, and a capacitive coupling voltage from the common electrode are allowed to have a distribution in a screen, whereby flickering and a brightness gradient are corrected simultaneously (Col. 11, Lines 57 –67, Col. 12, Lines 55-64, Col. 8, Lines 55 to Col. 9, Line 37).

Regarding Claim 56, Yoshida et al. teaches a display apparatus (Col. 8, Line 39) comprising: a plurality of pixel electrodes (Col. 6, Line 48) arranged in a matrix (Col. 6, Line 36); switching elements connected thereto (Col. 6, Line 42); scanning electrodes (Col. 6, Lines 64, 23-25), video signal electrodes (Col. 7, Line 5-7, Col. 6, Lines 25-27); common electrodes (Col. 6, Line 55,56); a counter electrode (Col. 6, Lines 55,56, Lines 12,13); a display medium

interposed between the pixel electrodes and the counter electrodes (Col.6, Lines 9-16); and storage capacitance formed between the pixel electrodes (Col. 6, Lines 54-57, Col. 7, Lines 14-26) and the common electrodes (Col. 6, Lines 55-56), wherein a plurality of the common electrodes that are connection destinations of the storage capacitance are connected to the pixel electrodes of a plurality of pixels belonging to one of the scanning electrodes (Col. 6, Lines 22-50).

Regarding Claim 57, Yoshida et al. teaches a display apparatus (Col. 8, Line 39) comprising: a plurality of pixel electrodes (Col. 6, Line 48) arranged in a matrix (Col. 6, Line 36); switching elements connected thereto (Col. 6, Line 42); scanning electrodes (Col. 6, Lines 64, 23-25), video signal electrodes (Col. 7, Line 5-7, Col. 6, Lines 25-27); common electrodes (Col. 6, Line 55,56); a counter electrode (Col. 6, Lines 55,56, Lines 12,13); a display medium interposed between the pixel electrodes and the counter electrodes (Col.6, Lines 9-16); and storage capacitance formed between the pixel electrodes (Col. 6, Lines 54-57, Col. 7, Lines 14-26) and the common electrodes (Col. 6, Lines 55-56), wherein a plurality of the common electrodes oppose the pixel electrodes of a plurality of pixels belonging to one of the scanning electrodes via the display medium (Col. 6, Lines 9-16, 52-60).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (6,496,170 B1) in view of Takubo (6,040,813).

Regarding Claim 58, Yoshida et al. teaches a display apparatus (Col. 8, Line 39) comprising: a plurality of pixel electrodes (Col. 6, Line 48) arranged in a matrix (Col. 6, Line 36); switching elements connected thereto (Col. 6, Line 42); scanning electrodes (Col. 6, Lines 64, 23-25), video signal electrodes (Col. 7, Line 5-7, Col. 6, Lines 25-27); common electrodes (Col. 6, Line 55,56); a counter electrode (Col. 6, Lines 55,56, Lines 12,13); a display medium interposed between the pixel electrodes and the counter electrodes (Col.6, Lines 9-16); and storage capacitance formed between the pixel electrodes (Col. 6, Lines 54-57, Col. 7, Lines 14-26) and the common electrodes (Col. 6, Lines 55-56),

However, Yoshida et al. fails to teach a scanning electrode - pixel electrode capacitance between the pixel electrodes and the scanning electrodes is represented by Cgd , a common electrode - pixel electrode capacitance between the pixel electrodes and the common electrodes is represented by Cst and a total capacitance connected electrically to the pixel electrodes is represented by Ctot, agd, and ast represented by agd = Cgd/Ctot ast = Cst/Ctot are set to be different values between a portion close to feeding ends in a screen and a portion away therefrom.

However, Takubo teaches a scanning electrode - pixel electrode capacitance between the pixel electrodes and the scanning electrodes is represented by Cgd , a common electrode - pixel electrode capacitance between the pixel electrodes and the common electrodes is represented by

Cst (Col. 4, Line 63 to Col. 5, Line 14) and a total capacitance connected electrically to the pixel electrodes is represented by Ctot (Col. 5, Lines 62,66), agd and ast represented by agd = Cgd/Ctot, ast = Cst/Ctot (Col. 5, Lines 62-66) are set to be different values between a portion close to feeding ends in a screen and a portion away therefrom (it is well known to one in the ordinary skill in the art the wiring capacitance gets added to the scan line and data line depending on how far they are from one end screen to the other end of screen and also how far the signal driver are located that are feeding the signal to scan line and video signal lines. The value of storage capacitance are set and gate to drain capacitance are also set values different than storage to offset the effect of the wiring capacitance which would make greater difference).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Takubo teaching in teaching of Okada et al. to be able have low power consumption, to control of uniformity of display and to produce high quality image.

6. Claims 1-3, 43,44,47-49,64,65,67-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. (5,561,442) in view of Takubo (6,040,813).

Regarding Claim 1, Okada et al. teaches a display apparatus (Col. 1, Line 14,15), comprising: a plurality of pixel electrodes arranged in a matrix (Col. 1, Lines 15,16); switching elements connected thereto (Col. 1, Lines 30-32); scanning electrodes (Col. 1, Lines 22-24); video signal electrodes (Col. 1, Lines 24-26); common electrodes (Col. 1, Line 21); a counter electrode (Col. 1, Line 20); a display medium interposed between the pixel electrodes and the counter electrode (Col. 1, Lines 14-20, Lines 34-38); and storage capacitance formed between

the pixel electrodes and the common electrodes (Col. 1, Lines 38,39, Col. 6, Lines 25,26), wherein, in a case where a scanning electrode - pixel electrode capacitance between the pixel electrodes and the scanning electrodes is represented by Cgd (figure 1, Col. 6, Lines 30,31), a common electrode - pixel electrode capacitance between the pixel electrodes and the common electrodes is represented by Cst (figure 1, Col. 6, Lines 25,26, Col. 1, Lines 35-37).

However, Okada et al. fails to teach a total capacitance connected electrically to the pixel electrodes is represented by Ctot, agd and ast represented by agd = Cgd/Ctot, ast = Cst/Ctot are set to be different values between a portion close to feeding ends in a screen and a portion away therefrom.

However, Takubo teaches a total capacitance connected electrically to the pixel electrodes is represented by Ctot (Col. 5, Lines 62,66), agd and ast represented by agd = Cgd/Ctot, ast = Cst/Ctot (Col. 5, Lines 62-66) are set to be different values between a portion close to feeding ends in a screen and a portion away therefrom (it is well known to one in the ordinary skill in the art the wiring capacitance gets added to the scan line and data line depending on how far they are from one end screen to the other end of screen and also how far the signal driver are located that are feeding the signal to scan line and video signal lines. The value of storage capacitance are set and gate to drain capacitance are also set values different than storage to offset the effect of the wiring capacitance which would make greater difference).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Takubo teaching in teaching of Okada et al. to be able have low power consumption, to control of uniformity of display and to produce high quality image.

Regarding Claim 2, Okada et al. teaches a video signal driving circuit for applying two kinds of video signals having different polarities to video signal electrodes in accordance with a display period (Col. 9, Lines 45-49).

Regarding Claim 3, Okada et al. teaches a common electrode potential control circuit for applying a voltage signal to a plurality of common electrodes and a scanning signal driving circuit, for applying a voltage signal to a plurality of scanning electrodes, the common electrode potential control circuit has output potential levels of at least two values, and the scanning signal driving circuit has output potential levels of at least two values (Col. 9, Lines 18-23, Line 60 to Col. 10, line 2, Col. 10, Lines 26-42).

Regarding Claim 43, Okada et al. teaches the display medium is liquid crystal (Col. 1, Line 10-12).

Regarding Claim 44, Okada et al. teaches a configuration forming a parallel plate capacitance in which a liquid crystal layer is interposed between the pixel electrodes and the counter electrode (Col. 1, Lines 40-45, Col. 6, Line 25).

Regarding Claim 47, Takubo teaches at least one of capacitances forming Ctot, includes a capacitance formed by two conductive layers or semiconductor layers sandwiching an insulating layer there between, and an overlapping area of the two conductive layers or semiconductor layers is made different between the portion close to the feeding ends in the screen and the

portion away therefrom (Col. 4, Line 48 to Col. 5, Line 18), whereby ast or alc and agd are allowed to have different values between the portion close to the feeding ends in the screen and the portion away therefrom (Col. 5, Lines 62-66) are set to be different values between a portion close to feeding ends in a screen and a portion away therefrom (it is well known to one in the ordinary skill in the art the wiring capacitance gets added to the scan line and data line depending on how far they are from one end screen to the other end of screen and also how far the signal driver are located that are feeding the signal to scan line and video signal lines. The value of storage capacitance are set and gate to drain capacitance are also set values different than storage to offset the effect of the wiring capacitance which would make greater difference).

Regarding Claim 48, Okada et al. teaches after a potential is written to the pixel electrodes via the switching elements, a voltage is superimposed via Cs, and has a value different between the portion close to the feeding ends in the screen and the portion away therefrom (Col. 4, Lines 40-50, (it is well known to one in the ordinary skill in the art the wiring capacitance gets added to the scan line and data line depending on how far they are from one end screen to the other end of screen and also how far the signal driver are located that are feeding the signal to scan line and video signal lines. The value of storage capacitance are set and gate to drain capacitance are also set values different than storage to offset the effect of the wiring capacitance which would make greater difference).

Regarding Claim 49, Okada et al. teaches when a scanning electrode is selected, a first potential level Vc(+) is applied to common electrodes that are connection destinations of storage

capacitance connected to pixel electrodes of a plurality of pixels belonging to the scanning electrode in a case where a polarity of a video signal is positive and a second potential level Vc (-) is applied thereto in a case where a polarity of the video signal is negative (Col. 9, Line 18 to Col. 10, Line 3, Col. 12, Line 58 to Col. 13, Line 8).

Regarding Claim 64, Okada et al. teaches a common electrode potential is different between a retention period after the pixel electrodes are charged with a positive video signal and a retention period after the pixel electrodes are charged with a negative video signal (Col. 1, Line 61 to Col. 2, line 8Col. 5, Lines 5-25, Col. 9, Line 18 to Col. 10, Line 3, Col. 12, Line 58 to Col. 13, Line 8).

Regarding Claim 65, Okada et al. teaches the scanning signal driving circuit conducts writing to a plurality of lines simultaneously (Col. 1, Lines 27-33, Col.4, Lines 37-50).

Regarding Claim 67, Okada et al. teaches the scanning signal driving circuit and the common electrode potential control circuit are formed on the same substrate as that of the switching elements (Col. 4, Lines 17-26).

Regarding Claim 68, Okada et al. teaches the display medium is composed of a medium is whose optical state is controlled with a current and auxiliary switching elements (Col. 4, Lines 17-26).

Regarding Claim 69, Okano et al. teaches the medium whose optical state is controlled with a current is an organic electro-luminescence medium (Col. 5, Lines 27-49, Col. 16, Lines 6-23).

7. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. (5,561,442) in view of (6,040,813) applied to claims 1-3, 43,44,47-49,64,65,67-69 above, and further in view of Okano et al. (5,600,458).

Regarding Claim 66, Okada et al. teaches a display apparatus (Col. 1, Line 14,15), comprising: a plurality of pixel electrodes arranged in a matrix (Col. 1, Lines 15,16); switching elements connected thereto (Col. 1, Lines 30-32); scanning electrodes (Col. 1, Lines 22-24); video signal electrodes (Col. 1, Lines 24-26); common electrodes (Col. 1, Line 21); a counter electrode (Col. 1, Line 20); a display medium interposed between the pixel electrodes and the counter electrode (Col. 1, Lines 14-20, Lines 34-38).

However, Okada et al. fails to teach specifically the display medium is liquid crystal of an OCB mode.

However, Okano et al. teaches the display medium is liquid crystal of an OCB mode (Col. 5, Lines 27-49, Col. 16, Lines 6-23).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Okano et al. teaching in teaching of Okada et al. to be able to achieve high resolution and high contrast display.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references either anticipate or render the claims obvious. In order to not to be repetitive and exhaustive, the examiner did draft additional rejection based on those references.

Allowable Subject Matter

9. Claims 4-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

a potential of a scanning electrode becomes a first potential level Vgon when the scanning electrode is selected and becomes substantially a second potential level Vgoff during a retention period in which the scanning electrode is not selected, a potential of a common electrode that is a connection destination of storage capacitance connected to pixel electrodes of a plurality of pixels belonging to the scanning electrode becomes a first potential level Vc(+) in a case where a polarity of a video signal is positive and a second potential level Vc(-) in a case where the polarity of the video signal is negative, when the scanning electrode is selected, and in a case where a difference between the first potential level Vc(+) of the common electrode and a potential during a subsequent retention period is represented by ?Vc(+), and a difference between the second potential level Vc(-) of the common electrode and a potential during a subsequent retention period is represented by ?Vc(-), **? represented by ? = astVcp/2 (where Vcp =**

AVc(+)-Avc(-)) is set to be smaller in the portion away from the feeding ends in the screen, compared with the portion close thereto and assuming that a value of y in the portion close to the feeding end; in the screen is y(O), a value of yin the portion away from the feeding ends in the screen is y(E), and a value of yin a portion in a middle there between in terms of a distance is y(4), y(M) is smaller than [y(O) +y(E)]/2 and Vcp takes a negative value and B = agd + ast (AVcc/AVgon) (where AVgon = Vgon - Vgoff, AVcc = [AVc(+) + AVc(-)]/2 is set to be larger in the portion away from the feeding ends in the screen, compared with the portion close thereto and a value of B in the portion close to the feeding ends in the screen is B(O), a value of B in the portion away from the feeding ends in the screen is B(E), and a value of B a portion in a middle there between in terms of a distance is B(M), B(M) is larger than [B(O) + B(E)]/2 and AVcc is negative and y represented by y = astVcp/2 (where Vcp = AVc(+) – Avc(-) is set to be smaller in the portion away from the feeding ends in the screen, compared with the portion close thereto, and B represented by B = agd + ast (AVcc/AVgon) (where AVgon= Vgon- Vgoff, AVcc = [AVc(+) + AVc(-)]/2 is set to be larger in the portion away from the feeding ends in the screen, compared with the portion close thereto.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Okada et al. (5,561,442) Method and circuit for driving a display device.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2673

April 29, 2004

VIJAY SHANKAR
PRIMARY EXAMINER